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## CONFIGURABLE TWO DIMENSIONAL AND THREE DIMENSIONAL ELECTRICAL PACKAGING SYSTEM

### FIELD OF THE INVENTION

**[0001]** The present invention relates generally to packaging of integrated circuits. In particular, the present invention relates to the packaging of integrated circuits in a two- or three-dimensional structure using an optical interconnect system.

### BACKGROUND OF THE INVENTION

**[0002]** In the continuing efforts to reduce costs and increase performance of electronic computers, tailored, compact arrangements of electronic circuits are desirable. By minimizing the area dedicated to electronic circuitry, the distance over which electrical signals must travel is reduced, as are the material costs. Typically, space-saving minimization is achieved by fabricating, on a given area of a semiconductor chip, as many electronic circuits as feasible within a given fabrication technology. The resulting dense chips are generally disposed on the surface of a substrate in a side-by-side arrangement with space left in between to provide regions for electrical conductors that provide electrical interconnection for the chips. The chip contact locations can be electrically interconnected to substrate contact locations by means of wires bonded in between the chip contact location and substrate contact locations. Alternatively, the semiconductor chips may be mounted in a flip-chip configuration wherein an array of contact locations on the semiconductor chip is aligned and electrically interconnected with an array of contact locations on a substrate by means of solder mounds disposed between corresponding chips and substrate contact locations.

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**[0003]** In the microelectronics industry, integrated circuits, such as semiconductor chips, are mounted onto packaging substrates to form modules. In high performance computer applications, the modules contain a plurality of integrated circuits and are mounted onto a second level of packages, such as a printed circuit board or card.

**[0004]** As the performance requirements of computer applications, for example, continue to increase, the signal propagation time among modules and among chips, and even between individual devices on the chips becomes critical. Currently, chips are positioned together on a planar substrate and combined with circuits onto the substrate using insulators between wiring layers. To optimize signal propagation time, the distance between chips and circuits, as well as the dielectric constants of the insulators, are all minimized.

**[0005]** Despite the efforts in optimizing traditional architectures, it is apparent that these chip architectures will not allow desired performance levels in future generation machines. One significant factor in achieving desired performance is the time required for a signal to propagate long distances. Three-dimensional packaging structures address the problem of the signal propagation distances suffered by planar packages, but the difficulty has been finding a suitable way to interconnect the devices in a three-dimensional structure.

**[0006]** In U.S. Patent No. 5,848,214, entitled, "Optically-guiding multichip module", a Fiber Optic Plate is the substrate or part of the substrate in a multichip module. Multichip modules can be stacked to form layers of densely packed integrated circuit dice. Optical signals, guided by the fiber optic plate, carry data from one layer in the stack to one or more of the other multichip module layers or to peripheral devices physically separate from the stack.

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**[0007]** The '214 patent discloses optical fibers as providing an optical interconnect. By interconnecting layers with optical fiber, components can not be removed or exchanged for upgrading or optimizing the system operation. In addition, the system disclosed on the '214 patent requires alignment using an external apparatus such as a position-sensing optical detector.

**[0008]** A compact multi-chip module is described in U.S. Patent No. 6,426,559 titled "Miniature 3D multi-chip module." The multi-chip module may be built from a lead frame that does not have a die attach pad. Instead, the leads of the lead frame may define a central opening. A first semiconductor device extends across the central opening and is connected to the plurality of leads, with the leads being on a first side of the first semiconductor device. A second semiconductor is stacked on the first side of the first semiconductor device. A third semiconductor device is stacked on the second semiconductor device. A fourth semiconductor device is stacked on the third semiconductor device. The stack of semiconductor devices passes through the central opening formed by the plurality of leads. The stack of semiconductor devices is encapsulated with a thermoset plastic. The resulting final assembly may occupy no more volume than a typical single chip component.

**[0009]** A multi-stack 3-D semiconductor structure is described in U.S. Patent No. 6,451,634 titled "Method of fabricating a multi-stack 3-dimensional high density semiconductor device." The multi-stack 3-D semiconductor structure described comprises a first level structure comprising a first semiconductor substrate and first active devices; and a second level structure comprising a SOI semiconductor structure bonded to the first level structure and further comprising second active devices; and wherein the first active

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devices are more heat tolerant than the second active devices is provided along with a method for its fabrication.

**[0010]** An optoelectronic integrated circuit device is described by U.S. Patent No. 6,396,967 titled "Optoelectronic integrated circuit device." The disclosed optoelectronic integrated circuit device is reported to have less signal damping and signal transmission loss, and includes a first optoelectronic integrated circuit and a second optoelectronic integrated circuit. Each of the first and second optoelectronic integrated circuits includes an electric circuit unit, an optical output terminal unit, and an optical input terminal unit. The first optoelectronic integrated circuit and the second optoelectronic integrated circuit are arranged so that each optical output terminal unit faces each corresponding optical input terminal unit. In this arrangement, light signal transmission can be carried out between a plurality of optoelectronic integrated circuit devices. Thus, signal damping and transmission loss can be reduced, and signal transmission delay time can be shortened.

**[0011]** A hermetically sealed package for at least one semiconductor chip is described by U.S. Patent No. 6,320,257 titled "Chip packaging technique." The hermetically sealed package is formed of a substrate having electrical interconnects thereon to which the semiconductor chips are selectively bonded, and has a lid which preferably functions as a heat sink, with a hermetic seal being formed around the chips between the substrate and the heat sink. The substrate is formed of or includes a layer of a thermoplastic material having low moisture permeability which material is preferably a liquid crystal polymer (LCP) and is a multiaxially oriented LCP material for preferred embodiments. Where the lid is a heat sink, the heat sink is formed of a material having high thermal conductivity and preferably a coefficient of thermal expansion, which substantially matches that of the chip. A hermetic bond is formed between the side of

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each chip opposite that connected to the substrate and the heat sink. The thermal bond between the substrate and the lid/heat sink may be a pinched seal or may be provided, for example by an LCP frame which is hermetically bonded or sealed on one side to the substrate and on the other side to the lid/heat sink. The chips may operate in the RF or microwave bands with suitable interconnects on the substrate and the chips may also include optical components with optical fibers being sealed into the substrate and aligned with corresponding optical components to transmit light in at least one direction. A plurality of packages may be physically and electrically connected together in a stack to form a 3D array.

**[0012]** A three-dimensional packaging architecture is described by U.S. Patent No. 6,268,238 titled "Three dimensional package and architecture for high performance computer." This patent discloses a three-dimensional packaging architecture for ultimate high performance computers and methods for fabricating circuits according to the architecture. The package allows very dense packaging of multiple integrated circuit chips for minimum communication distances and maximum clock speeds of the computer. The packaging structure is formed from a plurality of subassemblies. Each subassembly is formed from a substrate, which has on at least one side thereof at least one integrated circuit device. Between adjacent subassemblies there is disposed a second substrate. There are electrical interconnection means to electrically interconnect contact locations on the subassembly to contact locations on the second substrate. The electrical interconnection means can be solder mounds, wire bonds and the like. The first substrate provides electrical signal intercommunication between the electronic devices and each subassembly. The second substrate provides ground and power distribution to the plurality of subassemblies. Optionally, the outer surfaces of the structure that can be disposed a cube of memory chips.

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**[0013]** General purpose methods for the fabrication of integrated circuits from flexible membranes formed of very thin low stress dielectric materials are described by U.S. Patent No. 5,637,907 titled "Three dimensional semiconductor circuit structure with optical interconnection." The flexible membranes are formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers. Semiconductor devices are formed in a semiconductor layer of the membrane. The semiconductor membrane layer is initially formed from a substrate of standard thickness, and all but a thin surface layer of the substrate is then etched or polished away. In another version, the flexible membrane is used as support and electrical interconnect for conventional integrated circuit dice bonded thereto, with the interconnect formed in multiple layers in the membrane. Multiple dice can be connected to one such membrane, which is then packaged as a multi-chip module. Other applications are based on (circuit) membrane processing for bipolar and MOSFET transistor fabrication, low impedance conductor interconnecting fabrication, flat panel displays, maskless (direct write) lithography, and 3D IC fabrication.

**[0014]** A structure for packaging electronic devices is described in U.S. Patent No. 5,531,022 titled "Method of forming a three dimensional high performance interconnection package." The structure for packaging electronic devices, such as semiconductor chips, in a three dimensional structure permits electrical signals to propagate both horizontally and vertically. The structure is formed from a plurality of assemblies. Each assembly is formed from a substrate having disposed on at least one surface a plurality of electronic devices. Each assembly is disposed in a stack of adjacent assemblies. Between adjacent assemblies there is an electrical interconnection means electrically interconnecting each assembly. The electrical interconnection means is formed from an elastomeric interposer. The elastomeric interposer is formed from an elastomeric material having a plurality of

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electrical conductors extending therethrough, either in a clustered or un-clustered arrangement. The electrical interconnection means is fabricated having a plurality of apertures extending therethrough. The array of apertures corresponds to the array of electronic devices on the substrates. The aperture and electrical interconnection means are disposed over the array of electronic devices so that the electrical interconnection means is between adjacent electronic devices. The stack of assemblies is compressed thereby compressing the electrical interconnection means between adjacent assemblies. The substrate or each assembly is formed from a thermally conductive material such as diamond. A heat dissipation means is thermally connected to the edges of the substrate to extract heat generated within the structure. Methods for fabricating the electrical interconnection means as a stand-alone elastomeric sheet are described. The ends of the plurality of conductors in the electrical interconnection means are fabricated so that upon compression between adjacent assemblies there is a wiping action between the conductor ends and contact locations on the adjacent assemblies to form a good electrical contact therewith.

**[0015]** An apparatus connecting electrical circuit boards is described in U.S. Patent No. 6,304,690 titled "Connecting a plurality of circuit boards." The apparatus connects electrical circuit boards (1, 2, 3, . . . N) so each board can communicate with every other board. Each board has an optical circuit, which in turn has a transmitter module (T) and a receiver module (R). The transmitter module (T) has electrical to optical converters (11B) for converting electrical signals into optical signals, a wavelength multiplexer (12) for multiplexing the optical signals into a single optical waveguide (12A), and an optical splitter (13) for dividing the multiplexed signal into a plurality of identical signals for transmission to each of the receiver modules (R). The receiver module (R) has an optical selector (14) for selecting signals from the transmission modules (T), a wavelength

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demultiplexer (21) for demultiplexing the selected signal into signals each of a different wavelength ( $\lambda_1 \dots \lambda_n$ ), and optical to electrical converters (22B) for converting each of the signals of different wavelengths into an electrical signal.

#### SUMMARY OF THE INVENTION

**[0016]** The present invention provides an integrated circuit module comprising an interconnect system extending from the exterior of the module. The interconnect system comprises a first connector and a second connector, wherein the first and second connectors are complementary connectors. The first connector comprises a first electrical connector and a first optical device, and the second connector comprises a second electrical connector complementary to the first electrical connector and a second optical device complementary to the first optical device. The first and second optical devices each comprise optical emitters and detectors.

**[0017]** In one embodiment of the invention, the integrated circuit module comprises third and fourth connectors, and the third and fourth connectors are complementary. In still another embodiment of the invention, the module further comprises a fifth and a sixth connectors, and the fifth and sixth connectors are complementary.

**[0018]** The present invention also provides an integrated circuit packaging apparatus comprising at least two integrated circuit modules. The modules are connected via an attachment between a first connector and a second connector, and each module comprises at least one first connector and at least one second connector. The first connector on a module adapted to form an attachment with the second connector on an

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adjacent module, the attachment providing a mechanical, an electrical, and an optical connection between the module and the adjacent module.

**[0019]** The present invention also provides a method of assembling an integrated circuit apparatus comprising interchangeably attaching at least two integrated circuit modules. In one embodiment, the method of assembling an integrated circuit apparatus comprises interchangeably attaching integrated circuit modules to form a two-dimensional array of interconnected integrated circuit modules. In another embodiment, the method comprises interchangeably attaching integrated circuit modules to form a three-dimensional array of interconnected integrated circuit modules.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

**[0021]** FIG. 1A is a perspective view of an integrated circuit module according to the invention.

**[0022]** FIG. 1B is a perspective view of two adjacent integrated circuit modules according to the invention.

**[0023]** FIG. 2A is a cross-sectional view of the module in FIG. 1A.

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**[0024]** FIG. 2B is a cross-sectional view of the modules in FIG. 1B.

**[0025]** FIG. 3 is a perspective view of a two-dimensional integrated circuit apparatus according to the invention.

**[0026]** FIG. 4 is a perspective view of a three-dimensional integrated circuit apparatus according to the invention.

**[0027]** Exemplary features of embodiments of the present invention are now described with reference to the figures. It will be appreciated that the invention is not limited to the embodiments selected for illustration. Rather, it is contemplated that any of the configurations and materials described below may be modified within the scope of this invention.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0028]** The present invention is directed towards two and three dimensional integrated circuit packaging systems utilizing modules that contain electrical and optical devices as building blocks. The modules are interconnected via an interconnect system to form integrated circuit architectures tailored to specific applications. The interconnect system of the present invention maximizes signal integrity and speed, thereby providing improved overall system performance. Furthermore, the 2D or 3D packaging system of the present invention provides versatility in fitting into unique and/or small architectural spaces.

**[0029]** The packaging system is constructed from basic units of integrated circuitry. These individual modules each have electrical and optical components embedded within

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them. The modules may be identical, or alternatively, the components may be customized so that the functionality of each module may differ.

**[0030]** As illustrated in FIG. 1A, the module 10, includes mechanical, electrical and optical interconnections. Specifically shown extending from the side of module 10, are several elements of the module that make-up the interconnection system. Specifically, two types of connectors are shown 214, 216. As described in more detail below, each connector comprises an electrical element and a mechanical element. Also shown are two types of optical elements, an optical emitter, or diode 220, and an optical detector 222.

**[0031]** The interconnect system elements on side 16 are complimentary to the elements extending from the orthogonal side 14. This complementariness is more clearly illustrated in FIG. 2A, which is the cross-sectional view of the module in FIG. 1A along the dotted line labeled A-A.

**[0032]** The view of FIG. 2A shows that the module 10 is formed of a substrate 210, which is formed of any conventional substrate material, such as ceramic, glass, Bakelite®, or epoxy. Embedded within each substrate 210 is a plurality of components 212. The type and number of components 212 embedded within each substrate 210 of each module 10 is user defined and customizable. Components 212 are representative of any logic function or device, such a microprocessor device, field programmable gate array (FPGA) or a memory device, useful in, for example, a computer application. The number and orientation of the electrical and optical connecting elements is exemplary. The electrical connection between one component 212 and another is accomplished via standard wiring or optical connections within substrate 210.

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**[0033]** As shown in FIG. 2A, the interconnect system 112 includes optical devices 18, 20. The optical devices are made up of a plurality optical elements, including optical emitters 220, which can be laser diodes, light emitting diodes, or other devices for emitting optical signals at any wavelength and a plurality of photo detectors 222. Photo detectors 222 may be conventional semiconductor devices, such as conventional photo diodes or photo transistors that generate electrical signals in response to light energy at any wavelength. The actual active device forming each emitter 220 may be embedded within substrate 210 and its light output is directed through the external surface of substrate 210 via a light transmission medium, such as an optical lens or an optical fiber. The devices 212 may be connected to the optical emitters 220 either directly or via a driver circuit (not shown). The devices 212 may be connected to the photo detectors 222 either directly or through a preamplifier circuit.

**[0034]** Photo detectors 222 provide variations in current or voltage as a function of received light intensity. The actual active device forming each photo detector 222 may be embedded within substrate 210 and its light input may be directed through the external surface of substrate 210 via a light transmission medium, such as an optical lens or a fiber optic element. Additionally, photo detectors 222 perform optical-to-electrical conversion for interfacing with electrical components 212.

**[0035]** The optical devices are arranged on or near the outer surfaces of substrate 210, as shown in FIG. 2A, and the precise number and arrangement of fasteners 214, 216, electrical conductors 218, photo emitters 220, and photo detectors 222 in the interconnect system may vary according to the desired application.

**[0036]** FIG. 2A also illustrates the fasteners 214, 216 of the interconnect system 112. These fasteners provide the electrical connectors of the interconnect system through

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electrical conductors 218. Fasteners 214, 216 are mechanical fasteners formed of, for example, ceramic, glass, metal, Bakelite®, or epoxy for interlocking one module to the next. As shown in FIG. 2A, fasteners 214a and 214b are positioned at the outer most edge of one side of substrate 210, while fasteners 214c and 214d are likewise positioned at the outer most edge of an adjacent side 14 of substrate 210. In contrast, fasteners 216a and 216b are positioned slightly inset from the outer most edge of side 16 of substrate 210, and fasteners 216c and 216d are likewise positioned slightly inset from the outer most edge of the adjacent side of substrate 210. This configuration demonstrates the complementariness of the fasteners; fasteners 214 are complementary to fasteners 216. Although not shown, it is contemplated that one or both of the fasteners 214 and 216 may have beveled edges to ease insertion of the fastener 216 into the fastener 214 and may also have latching surface to hold the fasteners together once they are joined. For example, each of the surfaces of the electrical conductors 218 may have a semicylindrical bump that engages with the bump on the complementary connector to hold the modules together while permitting them to be separated.

**[0037]** Alternatively, the fasteners 216 and 214 may be configured as shown with the non-metallic portion of the fasteners 216 and 214 providing a spring force that merges the electrical conductor portions 218 together when the fasteners 216 and 214 are joined in a press-fit configuration.

**[0038]** Table 1 provides example dimensions for a module 10 designed for use in a two-dimensional integrated circuit packaging system of the present invention.

Table 1

	Range	Specific example
Substrate <b>210</b> length	1 to 500 mm	20 mm
Substrate <b>210</b> width	1 to 500 mm	20 mm
Substrate <b>210</b> height	1 to 500 mm	20 mm
Fastener <b>214</b> length	0.1 to 50 mm	2 mm
Fastener <b>216</b> length	0.1 to 50 mm	2 mm
Optical interconnect system <b>112</b> pitch	0.1 to 50 mm	2 mm
Electrical conductor <b>218</b> thickness	0.1 to 100 $\mu\text{m}$	1 $\mu\text{m}$
Gap "g"	0 to 50 mm	2 mm

**[0039]** Complementary fasteners may be interlocked as illustrated in FIG. 2B. FIG. 2B shows the cross-sectional view along line B-B of FIG. 1B. FIG. 1B illustrates two modules 10a and 10b interconnected through the interconnect system. The two modules 10a, 10b are connected via an attachment 12 between the complementary connectors extending from the side of each module.

**[0040]** Details of the attachment are illustrated in FIG. 2B, which shows how the fasteners 214 and 216 are positioned to form an electrical connection. Each fastener has an electrical conductor element 218, and the electrical conductors make contact when an attachment is formed. Thus, in the example shown in the figures, the fasteners 216, 214 are electrical connectors between the modules. In this example, each inner surface of fasteners 214 and each outer surface of fasteners 216 contains an electrical conductor 218 for transferring electrical signals, including operational power signals, from one module 10a to the next 10b. Electrical conductors 218 may be formed from any electrically conducting material, such as copper or aluminum and may be gold plated to inhibit corrosion.

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**[0041]** When modules 10a, 10b are assembled within a packaging system 100, complementary optical devices 18 and 20 are positioned by the interconnect system attachment such that optical signals can be transmitted between the modules 10a and 10b. In FIG. 2B, the diodes 220 and photo detectors 222 are aligned permitting the light output of each diode 220 to be coupled to the input of an associated photo detector 222. This optical coupling propagates signals from one module 10 and the next interlocking module 10.

**[0042]** FIG. 2B generally illustrates how the elements of optical interconnect system 112 align and engage. The fasteners 216c and 216d of module 10b are engaged between fasteners 214c and 214d of module 10a. The electrical conductors 218 of fasteners 216c and 216d of module 10b are respectively in mechanical and electrical contact with electrical conductors 218 of fasteners 214c and 214d of module 10a. The fasteners serving as electrical connectors providing connections from electrical signals between from module 10a to module 10b. Generally, fasteners on any given module engage in like manner with fasteners of an adjacent module.

**[0043]** Similarly, FIG. 2B shows optical emitters 220 of module 10a aligned with photo detectors 222 of module 10b. Likewise, optical emitters 220 of module 10b are aligned with photo detectors 222 of module 10a. A gap  $g$  exists between the optical devices 20 and 18 when modules 10a and 10b are connected. Where  $g$  is greater than zero, the optical beam of emitters 220 is transmitted across free space. Signal transmission between adjacent modules is possible across the gap  $g$  via the optical devices within interconnect system 112. A microlens array either alone or combined with a diffractive optical element (DOE) may be used in order to enhance the propagation of optical signals between modules or in order to split the signal from one emitter and direct

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it to multiple receivers. A DOE is a diffractive element fabricated by conventional photolithography and etching technology commonly used in the silicon large-scale integration (LSI) industry. Utilization of a DOE in combination with a microlens array can allow the transmission distance between emitter and receiver to be extended over what could be achieved using a microlens alone. In this case, a DOE/microlens combination is positioned between emitters 220 and photo detectors 222. By using a microlens array, a packaging system with yet a smaller volume may be obtained.

**[0044]** Customization of the integrated circuit apparatus may be accomplished through customization of the individual modules or in combination with the assembly of multiple modules interconnected in the system. Thus, the packaging system provides for user-defined customization. For example, electrical conductors 218, emitters 220, and photo detectors 222 need not be oriented exactly as shown in the figures. Rather, these elements may differ in selection, number and location on the modules as determined by the specific application. The interconnections between the modules, for example, may form buses allows some signals to pass through the module to other modules. The interconnections may also be application configurable, depending on the designed use of the packaging system 100. Each emitters 220 and photo detector 222 is suitably placed on a surface of the module 10 to provide suitable communicate between modules. In one embodiment, suitable positions for optical coupling are determined automatically, without manual adjustment, by the height of fasteners 214 and 216. Additionally, modules are preferably easily detachable to enable the function within the total packaging system 100 to be easily changed. Because no leads are not necessary to establish electrical connections between modules, the architecture of the packaging system is environmentally conservative.

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**[0045]** Referring to FIG. 3, an example integrated circuit apparatus architecture formed from interconnected modules is illustrated. The packaging system 100 is a two-dimensional configuration of modules assembled into an integrated circuit packaging apparatus. The plurality of modules 110 that include electrical components 212 are designed according to any user-defined specifications depending on the overall desired function or application. Each module 110 is designed to fit within a specific X-Y location within the 2D packaging system. Accordingly, the modules have sets of interconnection systems extending to connect with adjacent modules. Each module 110 is oriented such that fasteners 214 of one module 110 are mechanically and electrically coupled to fasteners 216 of an adjacent module 110. Specifically, one side of module 110a is mechanically, electrically, and optically coupled to a first side of module 110b; one side of module 110e is coupled to a second side of module 110b; one side of module 110c is coupled to a third side of module 110b; and one side of module 110f is coupled to a fourth side of module 110b. Furthermore, a second side of module 110c is coupled to one side of module 110d. These multiple interconnections combine to form a single integrated circuit architecture shown in FIG. 3. The interconnect system allows flexibility in assembly the modules 110 in the X and Y planes. The interconnected modules allows operational power signals to be distributed from one module to the next via electrical connectors, and provides signal transmission from one module to the next via photo emitters and photo detectors.

**[0046]** Generally, the power distribution to each component 212 of a module is accomplished through electrical conductors from a power source (not shown). Furthermore, one or more components 212 may be power-generating devices using, for example, extracting power from either a magnetic field or an electric field, or may include specific energy exchanging components (e.g. a photo cell). Any heat generated by

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components 212 within each module may be dissipated by radiating to the surfaces of the module and subsequently removed via any cooling method, such as external fans. Additionally, heatsink devices (not shown) may be used within the packaging system 100. Furthermore, it is contemplated that if the interconnect system 112 is formed using heat conducting materials (e.g. diamond films) it may also serve as a heatsink.

**[0047]** As shown in FIG. 4, the interconnection system may be used to a form three-dimensional integrated circuit packaging apparatus. A perspective view of a exemplary 3D packaging system 300 is shown in FIG. 4. The 3D packaging system 300 includes a plurality of modules 310 arranged and electrically connected in the X-Y-Z planes. Modules 310 are connected by the optical interconnect system 312, which provides signal and power connections to adjacent modules in any orientation. More specifically, the 3D packaging system 300 of FIG. 4 includes modules 310a, 310b, 310c, 310d, 310e, 310f, 310g, and 310h arranged in one exemplary configuration. The packaging system is not limited to any particular configuration, as any number of modules can be arranged in any X-Y-Z arrangement.

**[0048]** Similar to the modules discussed above in the two dimensional configuration, each module 310 has electrical and/or optical components embedded within it. The components can vary to accommodate particular purposes, or be generic building block components (e.g. FPGA's) allowing the functionality of each module to be determined by the user. As a result, the function of modules 310 collectively within the 3D packaging system 300 is entirely customizable and user defined.

**[0049]** As apparent from FIG. 4, all six sides of each cubic module 310 may include the interconnect system extending from the exterior of the module. Mechanical, electrical, and optical interconnections are formed by the complementary interconnect systems on

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adjacent modules. The modules 310 are similar to modules 110 as described above. The key distinction between the modules being that all six sides of modules 310 have interconnect systems, whereas only four sides are equipped with the interconnect system on modules 110. Module 310 includes substrate 210 having electrical optical or electrooptic components 212 embedded therein, and the interconnect system 312 may be identical to optical interconnect system 112, as described in FIGS. 2A and 2B. Specifically, the interconnect system 312 includes fasteners 214, fasteners 216, electrical conductors 218, photo emitters 220, and photo detectors 222, as described in FIGS. 2A and 2B. Similarly, each photo emitter 220 and photo detector 222 may be suitably placed on the surface of a module 310 to allow communication between modules 310.

**[0050]** Similar to the modules 210 used in 2D architectures, the modules 310 may be designed according to any user-defined specifications depending on the overall desired function or application. Each module 310 may be designed to fit within a specific location within the 3D packaging system 300. The modules 310 are oriented within the 3D packaging system 300 to provide coupling through the interconnect systems to an adjacent module 310.

**[0051]** With reference to the example configuration of FIG. 4, one side of module 310a is mechanically, electrically, and optically coupled to a first side of module 310b; one side of module 310e is coupled to a second side of module 310b; one side of module 310c is coupled to a third side of module 310b; one side of module 310f is coupled to a fourth side of module 310b; one side of module 310g is coupled to a fifth side of module 310b; and one side of module 310h is coupled to a sixth side of module 310b.

**[0052]** Furthermore, a second side of module 310c is coupled to one side of module 310d. The result is a three-dimensional structure of integrated circuits. A variety of 3D

structures are obtainable by connecting modules 310. Power is distributed from one module to the next via electrical connectors of the fasteners and 216. Furthermore, signals are transmitted from one module to the optical devices.

**[0053]** Table 2 provides example dimensions for a module 310 designed for use in a three-dimensional integrated circuit packaging system according to the present invention.

Table 2

	<b>Range</b>	<b>Specific example</b>
Substrate <b>210</b> length	1 to 500 mm	20 mm
Substrate <b>210</b> width	1 to 500 mm	20 mm
Substrate <b>210</b> height	1 to 500 mm	20 mm
Fastener <b>214</b> length	0.1 to 50 mm	2 mm
Fastener <b>216</b> length	0.1 to 50 mm	2 mm
Optical interconnect system <b>312</b> pitch	0.1 to 50 mm	2 mm
Electrical conductor <b>218</b> thickness	0.1 to 100 $\mu\text{m}$	1 $\mu\text{m}$
Gap "g"	0 to 50 mm	0 mm

**[0054]** In summary, the 2D packaging system 100 and the 3D packaging system 300 of the present invention provide easily configurable electrical packaging. The system allows for unique 2D or 3D integrated circuit configurations by connecting modules. Furthermore, the use of optical coupling via photo emitters and photo detectors ensures maximum signal transmission speed and signal integrity beyond the capabilities of conventional wired interconnect systems, while minimizing EMI and crosstalk.

**[0055]** The architecture of the packaging systems is not limited to small components. The architecture principles apply generally to large substrates, for example,

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within a server or personal computer application. Additionally, while not illustrated in the figures, the modules may be of any multi-sided shape, for example, pyramidal or hexagonal, with the appropriate adjustment to the interconnect system components to maintain complementariness of adjacent modules.

**[0056]** Although the invention is illustrated and described herein with reference to specific embodiments, the invention is not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the invention.